

FIG. 1

FIG. 2

3/19

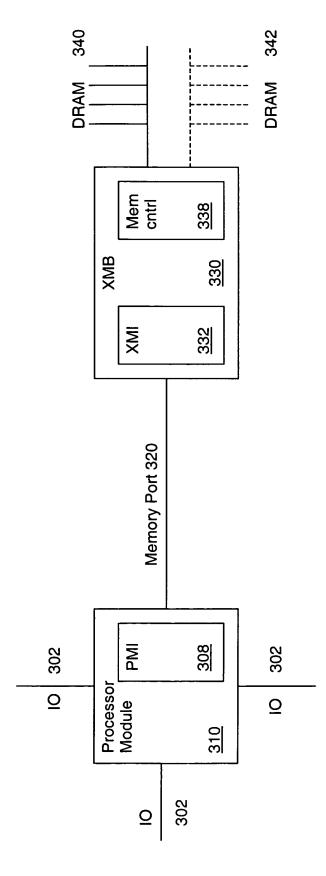


FIG. 3

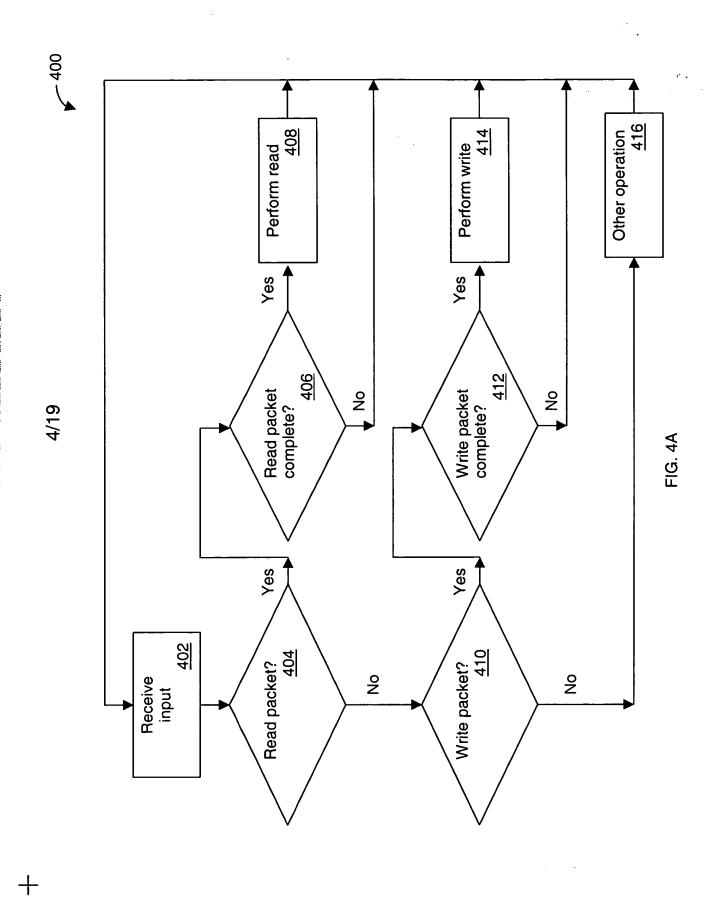


FIG. 4B

"H"D H"TO H"TO D 11 D1. WENT, Spirit St.

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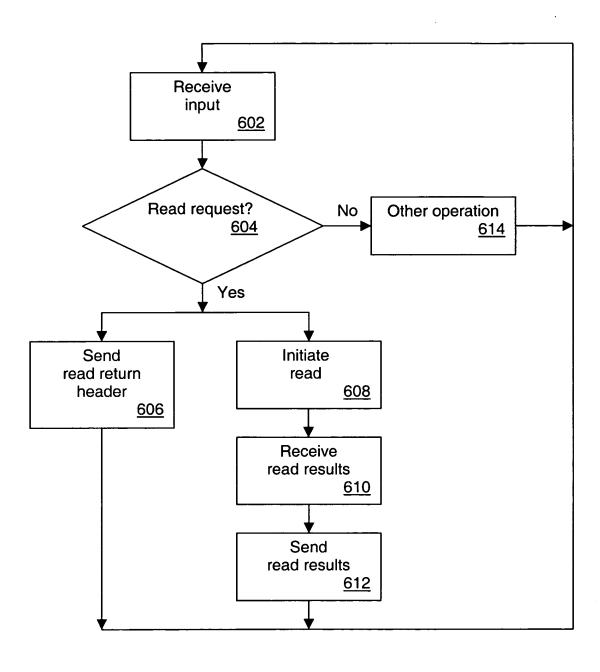


FIG. 6A

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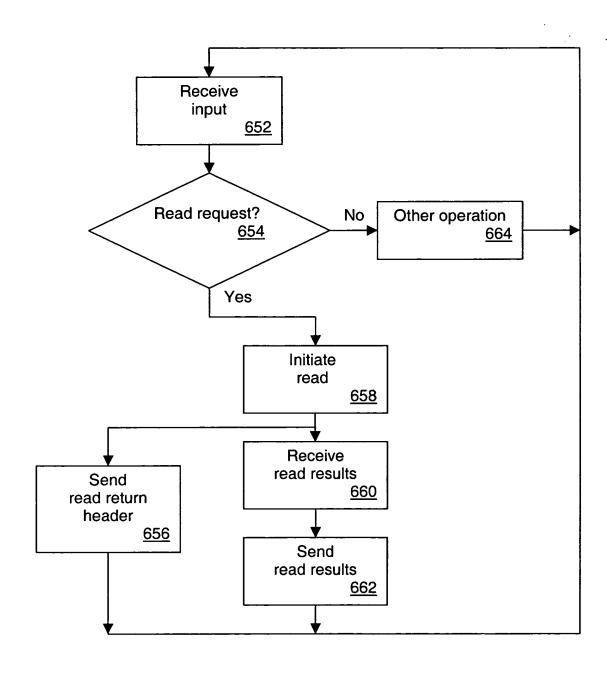


FIG. 6B

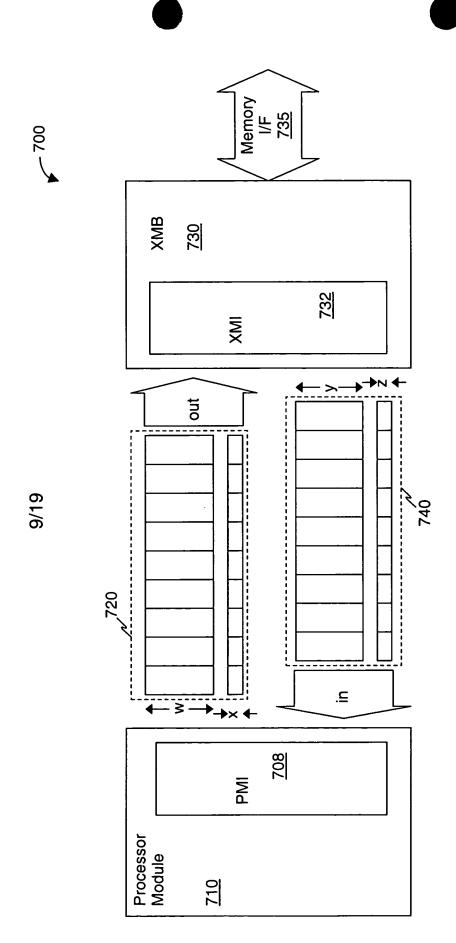


FIG. 7

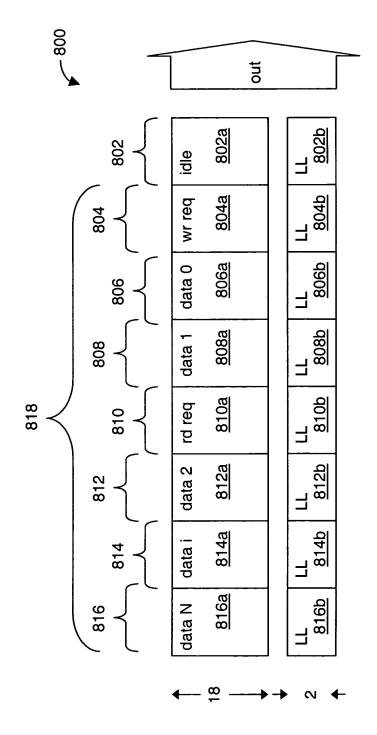


FIG. 8

+

FIG. 9

/ 1000			
*	←	₩	→ 4 ←
1016	data 0	<u>1016a</u>	LL 1016b
1014	data N	<u>1014a</u>	LL 1014b
1012	data i	1012a	1012b
1010	data 2	<u>1010a</u>	1010b
1008	data 1	1008a	1008b
1006	data 0	1006a	1006b
1004	idle	1004a	LL 1004b
1002	idle	1002a	1002b
_		.⊑	

FIG. 10

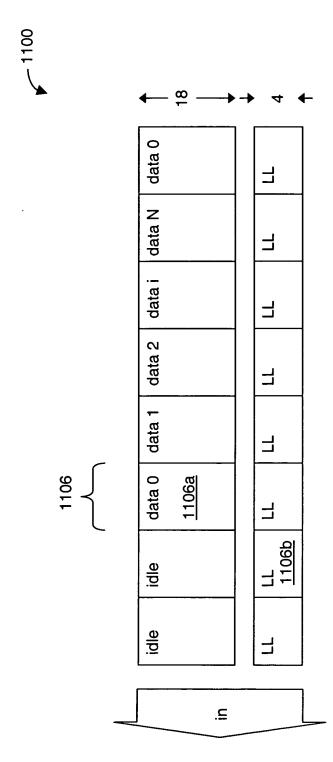


FIG. 11

7 1200

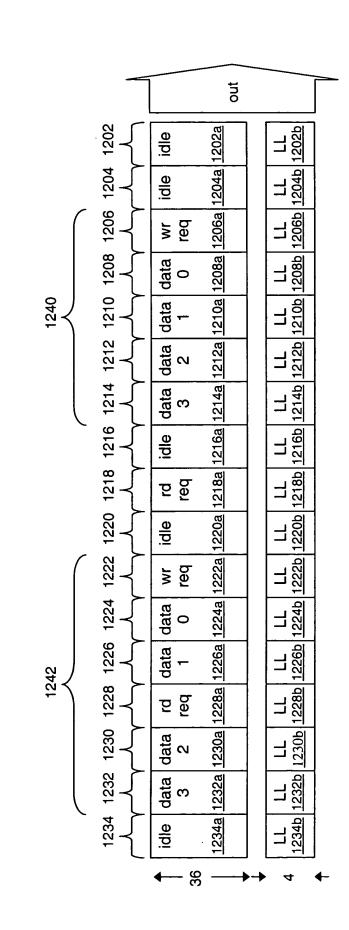


FIG. 12

	ite Command	ad Indicator	Check Bits, Mask Bits, Stream ID,	ity, etc.
BITS 17:0	Lower Order Address Bits and Read/Write Command	Higher Order Address Bits and Early Read Indicator	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Stream ID,	Size Bits, Cancel Command, Priority, etc.
↓Transfer	0	-	2	က

FIG. 13

√Transfer 0 1 2	BITS 17:0 Lower Order Address Bits and Read/Write Command Higher Order Address Bits and Early Read Indicator Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Size Bits, etc.
ო	

↓Transfer	BITS 17:0
0	Lower Order Configuration Address Bits and Read/Write Command
+	Higher Order Configuration Address Bits and Early Read Indicator
2	oto atianitation Office to Anna Andreas Transaction of State Mack Bits at
3	COMMINATION DESIMATION, OTISET MONESS, TRANSACTION ID, OTIECK DITS, MASK DITS, ETC.

FIG. 15

1600

LL signals	Transfers 0:3
0	Info and Check Bits
1	Header, Tail, and Check Bits
2	Extended Mode Bits
3	

FIG. 16

LL signals	Transfers 0:3
0	Type and Check Bits
1	Type and Oneck bits
2	Info and Check Bits
3	IIIIO and Check bits

FIG. 17



LL signals	Transfers 0:3
0	Tag Control and Chock Rits
1	Tag, Control, and Check Bits
2	Too Info and Chaok Dita
3	Tag, Info, and Check Bits

FIG. 18

1800

FIG. 19

2000

LL signal